

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A transistor circuit for implementing a switch, comprising:
 - a first switch node configured to connect to an external circuit;
 - a second switch node configured to connect to the external circuit;
 - a transistor device having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;
 - a third switch node for receiving the control signal; and
 - an impedance circuit connected to the third switch node and the third terminal of the transistor device, the impedance circuit configured with a sufficiently high impedance to reduce the effective parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch.

2. (previously amended) The transistor circuit of claim 1, wherein the transistor device is a metal-oxide-semiconductor field-effect transistor.

3-5. (cancelled)

6. (previously amended) A transistor circuit for implementing a differential switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a first transistor device having a first terminal connected to the first switch node, a second terminal, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;

a second transistor device having a first terminal connected to the second terminal of the first transistor device, a second terminal connected to the second switch node, and a third terminal configured to receive the control signal; and

a third transistor device having a first terminal connected to the first terminal of the first transistor device, a second terminal connected to the second terminal of the second transistor device, and a third terminal configured to receive the control signal, the third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit.

7. (original) The transistor circuit of claim 6, wherein the first transistor device, the second transistor device, and the third transistor device are each a metal-oxide-semiconductor field-effect transistor.

8-9. (cancelled)

10. (currently amended) The transistor circuit of claim 6, wherein the predetermined parasitic characteristics of the third transistor device reduce the effective parasitic resistance of the transistor circuit while sustaining a less than equivalent increase in effective parasitic capacitance of the transistor circuit.

11. (new) A transistor circuit for implementing a switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a transistor device having a first terminal connected to the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal for controlling the electrical connectivity between the first terminal and the second terminal; and

an inverter circuit connected to the second terminal of the transistor device for reducing the noise at the first terminal of the transistor device, the inverter circuit configured to:

pull the electrical connection of the second terminal of the transistor device to ground when the electrical connectivity of transistor device is enabled by the control signal; and

provide a voltage to the electrical connection of the second terminal of the transistor device when the electrical connectivity of the transistor circuit is not enabled by the control signal.

12. (new) The transistor circuit of claim 11, wherein the transistor device is a metal-oxide-semiconductor field-effect transistor.